

Broadband Power

Over the next five years, Power-One power management chips will transform the industry

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“What is the hottest development in semiconductors?” I was pondering my own choices—the optical “pins” from Stealthco or the seven layer network processors from EZchip (LNOP) or the Foveon super-high-resolution still and full-motion imager chip. But I had cornered a world-beating expert Derek Lidow, former head of **International Rectifier** (IRF) and president and CEO of **iSuppli**, the leading chip data boutique, on the back seat of a bus bouncing through the streets of Seoul. Perhaps he had a better idea.

As speakers headed for a celebration of Korean broadband technology at the Seoul Digital Forum early this month, we were undergoing narrowband butt-bruising travel in the back seat of the bus, where the signal-to-noise ratio dipped to the level of a streaming video over AOL.

“Digital Flower what?” I asked, with breakfast muesli lurching up my esophagus.

“**Power-One** (PWER),” answered Lidow. “They are digitizing power management chips. It will transform the industry. Some 50 percent of the revenues of all the analog chip companies, from **National Semiconductor** (NSM) to **Linear Technologies** (LLTC) to **International Rectifier**, come from power management. Working in stealth, Power-One has figured out how to digitize this function.”

The muesli tumbled back down to the pit of my stomach in an acidulous lump. “There goes my list,” I mumbled. “National, **Analog Devices** (ADI), **Texas Instruments** (TXN), all the rest will lose half their revenues?” I asked.

“Well, it won’t happen over night. But over the next five years, power management is going digital,” Lidow said.

Forty-dollar oil. Two-dollar gasoline. Crackling thunderstorms that dim lights and shut down computers at the *GTR*’s new Midwestern outpost and then roll east to crash our machines in the Massachusetts Berkshires. Power issues lend a new meaning to the concept of newsletter dead lines. Nurse your cellphone through to the beeping stage. Juggle the batteries for your digital camera. Cascade as many as three power-strip surge protectors and 10 AC-DC adaptors just to shield and serve a modest home office. Try to replace the photodetector in your driveway lamppost and get an unexpected shock. All around, daily events remind us of the centrality of energy, the importance of power management.

The digital economy now consumes some 14 percent of U.S. electricity. It is the chief source of new energy consumption. Even leading green guru James Lovelock, front line Cassandra for global warming, now admits we need nuclear power, and lots of it. Then there’s China. Accused of driving up the prices of coal and oil to meet its newly insatiable demand for energy, Beijing now plans to

build some 60 nukes—the peaceful kind. Can America much longer hold out on this miraculous but obvious source of cheap energy?

In the Telecom, power issues largely determine stock value. Taking over most of the cellphone industry and now preparing for dominance in computer networking as well, **Qualcomm** (QCOM) wins by mastering the inverse power law of electronics. CDMA (code division multiple access) prevails not only because of its intrinsic ten times greater power efficiency, but because of its superior digital power control. **Corvis** (CORV) all-optical networks win in part because they use far less power to route far more traffic. Less power per bit translates into less crosstalk and higher data rates.

From diesel-powered data centers at **Equinix** (EQIX) to **Intel's** (INTC) Pentium 4s with their cogeneration of office heating, power management is the thermostat of electronic architecture. The *GTR* has long favored analog semiconductor companies with expertise in power. National Semiconductor now calls itself a “power-management company.” Texas Instruments is the leader in the field, and Analog Devices is a major player, too. Two years ago we reasserted our view that analog specialists had an even brighter future than most chip companies, in part because of their unique place in what our friends Peter Huber and Mark Mills call the “powercosm.” Leading the NASDAQ over the last two years have been analog chip companies, and we regret not listing even more of them—**Linear Technologies** and **Maxim Integrated Products** (MXIM), to name two pure plays.

A hot industry

Power also drives the microeconomy of silicon. It dominates the ecology of transistors and gates and constrains the future of Moore's law. Power dissipated by a digital chip is proportional to the product of the capacitance, clock frequency, and the square of the input voltage (Power = Capacitance * Frequency * Voltage²). Voltage is like water pressure and currents resemble water flows. At a given power level, low voltages imply large currents across the ever-expanding millions of microchip gates. The analogy for current is the amount of water flowing through the pipes. Chips now operate at as much as 100 amps of current, which is enough to fuel 180 sixty-watt light bulbs. Broadband silicon thus does imply broadband power, in the sense that it requires a wide electronic medium to carry lots of current at a low voltage, and it takes a wide band of spectrum to carry lots of data at less-than-maxed-out bits-per-hertz.

In a world of fast processors running at hundreds of megahertz or gigahertz speeds, the easiest way to limit power is to reduce the squared term in the equation, voltage. Cut the voltage in half, and you can increase the clock frequency by a factor of four, retaining the same power dissipation. But you cannot keep reducing voltages forever; if

you do, transistors won't switch. Clock frequencies have gone up far more than voltages have dropped, and so chip wattage has increased dramatically, too. Because power is also the product of voltage and current ($P = I \cdot V$, where $I =$ current), as voltages drop and power increases, electrical currents must soar.

Famously illustrated by an Intel graph, power *densities*—power per unit area—are going through the roof. The Intel PowerPoint plot showed that heat generated by a Pentium long ago passed the “hot plate” stage and was on a line to achieve “nuclear reactor” status in the near future, then reach NASA “rocket-nozzle” levels sometime around 2010. Over the past decade, the crucial metric of power

Taking over most of the cell phone industry, Qualcomm wins by mastering the inverse power law of electronics

density has leapt by a factor of 4 for microprocessors in general, and by a factor of 10 for Pentiums. By 2005, a 200-million transistor chip built in a 65-nanometer process could waste 10 watts merely because of current leaking through transistors. Ten watts could run an entire CDMA base station.

Few people we know want rocket-nozzle laptops. So last winter Intel announced a new material that could replace silicon dioxide as the key transistor insulator. The company believes the material will reduce power consumption by limiting the current leakage of ever-small transistors with rapidly thinning walls. It will also require replacement of traditional polysilicon wires with new copper electrodes, a big change in the chip manufacturing process. It's just one among myriad physical, architectural, and software enhancements being pursued by hundreds of companies, all aiming to manage the power budget. **Novellus** (NVLS) is the leading player in the switch toward copper interconnects, though **Semitoool** (SMTL) is a purer play in the field.

There was a time not too long ago when almost all silicon ran on 5 volts. But in the nineties, as power considerations started to dominate chip and circuit-board design, chips moved down to 3.3V, then 2.5V, 1.5 V, 1V, and now .75V or even less. We can't reduce voltages forever, but the number of distinct supply voltages keeps increasing. Delivering the right current at the right voltage with increasing reliability has become a key challenge of the Telecom.

At the same time engineers started dropping voltages for large, fast chips, they also started putting more of these chips on the same circuit board. Microprocessors, digital signal processors (DSPs), field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), memory arrays—all need to be linked together to perform the intense real-time tasks of high-speed communications.

EZchip passes the test

What's an EZ investor to do? After hitting a 52-week peak of 12.17 in January, shares of Israel-based **EZchip** (LNOP) now trade at 6.25. The company said not to expect big revenues in the March quarter, but with more than 30 customers, many investors hoped for a surprise that did not come, and probably won't come in June either. A Nasdaq slump and Mideast angst on EZ's doorstep only added to the bearish mix.

Now this week comes John Chambers, CEO of imperial **Cisco** (CSCO), holding forth at the Computer History Museum in Mountain View. Flanked by an army of publicity privates, he is introducing the new HFR—known in polite company as the huge fast router. The product of four years of research and development, this half-million dollar, 14 kilowatt, 1.2 terabit, sixteen hundred pound machine was built to crush the competition. Scaling to 92 terabits, an HF network of HFRs can do it all: core, peering, aggregation, high-speed edge. It has new IOS-XR modular software and is designed to last in carrier networks for 20 years. What else do we need? Maybe the rest of Silicon Valley can take a two-decade holiday.

Compounding EZ worries is the fact that at the heart of Cisco's HF linecards are two **IBM** (IBM) manufactured ASICs dubbed silicon packet processors. Each contains one

hundred eighty-eight 32-bit RISC (reduced instruction set) processors, all executing specific tasks in massively parallel fashion. But you thought EZ's massively parallel merchant silicon was supposed to replace proprietary RISC-based ASICs in routers around the world. What's an EZ investor to do?

We'd say double down. Although Cisco has other router products, and routers overall comprise just 40 percent of its total business, this story seems to be following an all-too predictable pattern. Faced with disaggregation by smaller, faster, more specialized companies, Cisco is seeking new feats of high-end integration, scaling the heights of the carrier-grade performance ladder. EZchip's next generation NP-2 line, meanwhile, will move away from an IBM ASIC model to a much cheaper **Taiwan Semi** (TSM) system that could cut design and manufacturing costs in half. EZchip CEO Eli Fruchter wants to move down the food chain toward high volume applications. EZ is pursuing, and Cisco is shunning, Tredennick's law: *seek volume and you will achieve performance. Seek performance, and the volumes won't come.*

With some 35 customers at the end of the March quarter, EZ could easily boast 45 customers by year-end. Ten or 12 of them will be in production. No one knows how fast EZ's customer's routing and switching

products will sell, but EZ has \$19 million in cash to smooth any bumps in the road. With expenses of about \$2.5 million a quarter, that's two years worth of operation with no sales.

This week, low-end competitor **Motorola** (MOT) announced it would discontinue its C-Port network processor family. That leaves **Intel** (INTC) and **AMCC** as competitors, but AMCC does not have a 10-gigabit product in sight. Meanwhile EZchip was earning certification in IPv4, IPv6, and MPLS (multiprotocol label switching) in benchmark tests performed by the Tolly Group. Passing with flying wire-speed low-latency colors, EZ ran the tests using large, life-like routing tables of over a million routes for IPv4 and over half a million for IPv6. The only other 10-gigabit net processor to attempt the benchmark used just 135,000 IPv4 routes and 1,200 IPv6 routes. EZ is the only company to pass the LinleyBench tests, a related benchmark which adds DifServ to the equation, for IPv4 and MPLS.

Although EZ remains small and somewhat risky, as the customer list continues to grow we may have to change our line that the company is a daring "public venture capital play." With a market cap of just \$45 million, LNOP, which owns more than half of EZchip, still has venture-like upside potential.

— **Bret Swanson**

Tasks like routing and serving packets at 10 gigabits per second or transmitting and receiving 3G mobile phone signals result in a proliferation of power regimes. Each of these large, fast chips often needs its own highly reliable power source, usually supplying a unique voltage different from the rest of the circuit board and other chips. Bret needs 10 bulky black power adaptors just to run his home office. How can we provide individualized precision power

to multiple chips, all on a relatively small circuit board?

Brick layers

Increasingly, the preferred answer to this question comes from one company. Expert in the power arena for thirty years, Power-One has developed a new integrated board-level power system. It was the cynosure of the Applied Power Electronics Conference earlier this year in

TELECOSM TECHNOLOGIES

| | |
|--|--------------|
| Advanced Micro Devices | (AMD) |
| Agilent | (A) |
| Altera | (ALTR) |
| Analog Devices | (ADI) |
| Avanex | (AVNX) |
| Broadcom | (BRCM) |
| Cepheid | (CPHD) |
| Chartered Semiconductor | (CHRT) |
| Ciena | (CIEN) |
| Corvis | (CORV) |
| Energy Conversion Devices | (ENER) |
| Equinix | (EQIX) |
| Essex | (KEYW) |
| EZchip | (LNOP) |
| Flextronics | (FLEX) |
| Intel | (INTC) |
| JDS Uniphase | (JDSU) |
| Legend Group Limited | (LGHL.Y.PK) |
| McDATA | (MCDTA) |
| Microvision | (MVIS) |
| National Semiconductor | (NSM) |
| Power-One | (POWER) |
| Proxim | (PROX) |
| Qualcomm | (QCOM) |
| Samsung | (SSNLF/SSNH) |
| Semiconductor Manufacturing International | (SMI) |
| Sonic Innovations | (SNCI) |
| Sprint PCS | (PCS) |
| Synaptics | (SYNA) |
| Taiwan Semiconductor | (TSM) |
| Terayon | (TERN) |
| Texas Instruments | (TXN) |
| VIA Technologies | (2388.TW) |
| Wind River Systems | (WIND) |
| Xilinx | (XLNX) |
| Zoran | (ZRAN) |

Note: The Telecosm Technologies list featured in the *Gilder Technology Report* is not a model portfolio. It is a list of technologies that lead in their respective application. Companies appear on this list based on technical leadership, without consideration of current share price or investment timing. The presence of a company on the list is not a recommendation to buy shares at the current price. George Gilder and *Gilder Technology Report* staff may hold positions in some or all of the stocks listed.

ADVANCED FIBRE COMMUNICATIONS (AFCI)

ACCESS GLASS—FIBER TO THE CURB & PREMISES

MAY 27: 18.84, 52-WEEK RANGE: 14.98 – 27.50, MARKET CAP: 1.66B

Off the list. In January, AFCI was added to the *GTR* both as a “pure play in last mile optics” and because it had “purchased Marconi’s FTTC assets.” With Tellabs’s acquisition of AFCI, these reasons lose their significance. AFCI will become essentially a quarter of an old-world telecom supplier laden with Sonet and electronic baggage. Of late, Tellabs has been attempting to shift focus away from traditional circuit-based products toward IP and MPLS and also toward digital-edge technology. But Tellabs doesn’t have the all-optical vision of Ciena and Corvis, and last quarter over half of Tellabs sales were in digital crossconnects and related transport systems. So this month we remove AFCI from the list.

Avanex (AVNX)

MAGIC OF WAVELENGTH DIVISION MULTIPLEX (WDM)

MAY 27: 3.17, 52-WEEK RANGE: 2.50 – 7.57, MARKET CAP: 428.65M

To prove itself as the alternative to JDSU in optical components, the new Avanex (the former Corning, Alcatel, and Vitesse optical components divisions plus the old Avanex) has significant financial and structural hurdles to surmount.

Product-wise, Avanex is already JDSU2. Taking a broad-brush look, we see both companies in markets that range from enterprise and storage to cable to metro and long-haul, both offer components and modules and are working their way into subsystems, and both are in optical technologies that include transmission, amplification, dispersion compensation, multiplexing, and switching and routing.

On the financial side, however, the one similarity between Avanex and JDSU is that both have “craft-guild age” revenues of a paltry \$31,000 per employee. Otherwise, Avanex looks weak beside its more fiscally fit rival in four key areas:

1. Sales: Avanex’s are just 38% of JDSU’s communications sales and a mere 19% of JDSU’s total sales.
2. Gross margins: Avanex (21.0%), JDSU 25.0%
3. R&D as a percent of sales: Avanex a whopping 36.0%, JDSU 15.9%
4. SG&A as a percent of sales: Avanex (discounting \$2m due to restructuring) 36.4%, JDSU 22.0%

Avanex has only begun its integration plan (JDSU has been restructuring for several years); the March quarter was the second where results from the Corning, Alcatel, and Vitesse acquisitions were fully incorporated, giving us just one sequential quarter-to-quarter comparison. At the current rate, it takes Avanex 8 quarters to get a gross margin of 25 percent

to match JDSU, a company still reporting operating losses. To match JDSU proportionally, Avanex must improve cost of sales by 37.7%, R&D expenses by 55.2%, and SG&A by 39.6%.

On a bright note, beginning in the June quarter and going forward, Avanex should benefit significantly from Alcatel’s big win in the SEA-ME-WE 4 submarine network construction project which takes a route from southeast Asia through the Middle East to southern Europe. Alcatel stands to rake in more than half of the \$500m project, and Avanex has a 3-year agreement with Alcatel to supply 70 percent of their optical needs relating to Avanex products. (Also, as a majority shareholder in Avanex, Alcatel has a serious stake in Avanex’s success.) Undersea products generally command much higher gross margins than their terrestrial counterparts.

Ciena (CIEN)

OPTICS AND ACCESS TO FIBERSPHERE

MAY 27: 3.37, 52-WEEK RANGE: 3.12 – 8.14, MARKET CAP: 1.91B

Struggling Ciena has a long, uphill climb just to make a dollar. While revenues increased 12.5% sequentially to \$74.7m in the April quarter, gross margin plummeted from 31.5% to 11% due to an unfavorable product mix—revenues from higher-margin switching sales were pushed out and revenues from lower-margin deployments of long-haul systems were higher than expected.

Gross margin is expected to rebound to near 30% in the July quarter as sales increase by \$22.4m. But neither of these are true improvements: The Internet Photonics (optical Ethernet) and Catena (broadband access) acquisitions, which were completed the first few days of the July quarter, had been reported by Ciena to be generating combined quarterly revenues of about \$30m on their own. Hence, the expected revenue increase of \$22.4 million actually represents a revenue decrease of \$7.6m or 7.3% over the April quarter. As for gross margins, beginning in Q4 of 2002, Ciena had steadily improved them from the teens through the 20s to 31.2% and 31.5% respectively in the previous two quarters. So a return to 30% next quarter, including “higher margin Catena and IPI,” is not an improvement.

How precarious is Ciena’s situation? Assuming the company achieves its goal of reducing operating expenses to \$67.5m by Q1 of 2005, Ciena would need to triple revenues to \$225m to break even at 30% gross margin (assuming expenses in absolute dollars remain constant with significantly higher revenues) or increase gross margin to 42% at a more-than doubling of revenue to \$160m, Ciena’s projected sales break-even value.

R&D, at 62% of sales this quarter (lowest in over two years), is a killer. Ciena notes that, relative to com-

MEAD'S ANALOG REVOLUTION

NATIONAL SEMICONDUCTOR (NSM)
SYNAPTICS (SYNA)
SONIC INNOVATIONS (SNCI)

FOVEON
IMPINJ
AUDIENCE INC.
DIGITALPERSONA

COMPANIES TO WATCH

ATHEROS
ATI TECHNOLOGIES (ATYT)
BLUEARC
COX (COX)

CYRANO SCIENCES
ENDWAVE (ENWV)
ESS TECHNOLOGIES (ESST)
MEMORYLOGIX

NARAD NETWORKS
POWERWAVE (PWAV)
QUICKSILVER TECHNOLOGY
RF MICRO DEVICES (RFMD)

SEMITOOL (SMTL)
SIRF
SOMA NETWORKS
SYNOPSIS (SNPS)

petitors, they have invested more in core transport and switching products. Their strategy is to combine cut-backs with continued strong innovation to stay ahead technologically. However, in order to justify and sustain them, high R&D expenses must eventually bear the fruit of much higher revenues and margins.

To see its way through the long uphill climb to profits, Ciena has \$1.46b in cash and investments (but including \$690m in convertible notes); they burned just \$60m in the April quarter. Also, seeking new revenues in the face of the slow core-optical market, Ciena embarked on a last-mile broadband strategy by acquiring, this quarter, DSL and fiber-to-the-X vendor Catena Networks and optical Ethernet and WDM supplier Internet Photonics, after having expanded into multiprotocol edge devices with the WaveSmith acquisition of a year ago.

Corvis (CORV)

THE PARAMOUNT ALL-OPTICAL COMPANY

MAY 27: 1.45, 52-WEEK RANGE: 1.11 - 3.07, MARKET CAP: 703.68M

All bandwidth is not created equal. Corvis continues to prove that bandwidth is not a commodity, reporting during its April 30 quarterly conference call that its enterprise customers shop not only for price but also for quality, including time to set up new services. Those who disdain the all-optical vision, believing that all networks are identical, will shun Corvis after digesting MCI's latest revelation of its ever-increasing residential long-distance pricing problem. But MCI's optoelectronic links cannot compete with Broadwing on a price/quality/service metric, and Corvis continues to announce new enterprise customers apace, the latest being a "Fortune 500 company" that had been previously wedded to a "competitor" for "nearly a century." While MCI continues to report revenue erosion, sales from Broadwing's communications services have remained steady, with new enterprise customers offsetting losses in the consumer long-distance market. Look for revenues to rise in future quarters as Broadwing continues to take business away from its older and less nimble rivals.

Even prior to its Focal acquisition, to be completed later this summer, Corvis is already showing major improvements in its financials due to the Access Forward strategy to substantially lower access costs at the network edge, Corvis's major expense headache. Over just the past three quarters (the first ones to include figures from the Broadwing network), gross margins for communications services have increased from 23.4% to 31% and operating losses have decreased from (\$113.5m) to (\$29.4m).

Going forward, there will likely be a bump in the road when the Focal acquisition closes, due to restructuring costs and the administrative meshing of the two companies; Corvis will initially see a 50 percent

increase in its sales force, putting some pressure on SG&A. In the longer run, when synergies take hold, Focal will help increase gross margins yet further by controlling access costs and by lowering SG&A and increasing revenues through expanded service offerings.

JDSU (JDSU)

COMPONENTS GALORE FOR THE FIBERSPHERE

MAY 27: 3.35, 52-WEEK RANGE: 2.60 - 5.885, MARKET CAP: 4.82B

With \$79m in communications sales during the March quarter, JDSU is still the giant in optical components as measured both in revenues and product breadth, including markets ranging from enterprise and storage to cable to metro and long-haul networks and with product mix ranging from components to the often higher margin modules and circuit packs. As carriers continue their metro network build-outs and reduce inventories, JDSU is experiencing increasing demand for core-network products, which have surpassed 20% of communications sales.

However, JDSU's "other half," its commercial and consumer products group, is where the company really shines, with \$81m in revenues and continuing operating profits. This group boasts products for the medical, environmental, defense, aerospace, security, and biotech industries as well as perhaps the company's greatest opportunity, the fast-growing rear-projection and plasma display markets, where JDSU may be adding 4 new, major customers and where product development costs should be winding down over the coming year.

A confederation of acquisitions only two years ago, JDSU has made huge progress in unifying its operations and, with \$1.5b in cash and near cash and only \$464m in long-term debt, has a stellar balance sheet. But with a gross margin of 25% against SG&A and R&D expenses which alone sum to 38% of revenues, JDSU must significantly reduce its still burdensome cost of sales and operating expenses if it hopes to make any meaningful operating profits over the next one to two years.

On May 17, JDSU announced the purchase of privately-held E2O Communications for \$60m in cash. E2O develops and manufactures transceivers for the Ethernets (fast, gig, 10gig) and fibre channel and supports Sonet, ATM, and ESCON protocols.

JDSU entered datacom when it purchased IBM's transceiver business in Jan 2002 for \$100m cash plus 27m JDSU common shares. In addition to small form factor transceivers and gigE converters for SANs and LANs, the IBM acquisition gave JDSU expertise in low-cost packaging and assembly techniques that are critical for high-volume datacom applications.

So, what does JDSU gain with little E2O which reported just \$5m in sales during the last quarter? For one thing, seven new datacom customers. How much

of the \$5m in revenues do they represent? We don't know, and customers who overlap with JDSU may look elsewhere for a second source. JDSU also mentions additional expertise in "low-cost manufacturing ... greater economy scale ... other infrastructure cost synergies," in other words, the typical platitudes and essentially a repeat of the IBM announcement two years earlier.

What JDSU may really have been after is long-wavelength VCSEL technology. E2O may be one of only three companies to claim long-wavelength (1310 nm) VCSEL capabilities. E2O originally announced this breakthrough two years ago, and then again this past February. We hope that this time it is for real. As you would expect for a datacom manufacturer, most of E2O's transceiver products are 850 nm VCSELS, and their few 1310 nm offerings, as posted on the website, still used edge-emitter technology.

Why bother extending vertical technology (VCSEL stands for vertical cavity surface emitter laser) to longer wavelengths? VCSELS are easier to manufacture than edge-emitters: a thousand or so can be grown on a single wafer, and since they emit light out of their tops rather than their sides, they can be tested early on, while they're still on the wafer and before money has been spent on expensive packaging. VCSELS emit circular light beams, which are easier to couple to fiber than the elliptical output of edge-emitters. They also emit narrow linewidths, are cooler to run for higher reliability, and lase in only one transmission wavelength because of the short cavity-length. The longer cavities of edge-emitters lase over a dozen or more channels and "hopping" to unwanted wavelengths can become a problem.

VCSELS are inherently low-power devices. Resonating light vertically between mirrors results in a much shorter path through the gain medium when compared to edge-emitters, which resonate from side to side across the medium. But the power is good enough for datacom. With all the advantages, then, it is not surprising the VCSELS essentially replaced edge-emitters at 850 nm years ago.

Why has it taken so long to extend VCSELS to 1310 nm (and eventually 1500 nm)? Because different materials are needed to make the lasing mirrors at longer wavelengths, and these reduce power even further and also introduce manufacturing complexities that negate the advantages listed above for shorter wavelengths. So the question is, Has E2O overcome these obstacles to gain the VCSEL advantages over edge-emitters that have been the rule for years at 850 nm? Clearly, E2O and now JDSU think they have.

Power-One (PWER)

DIGITAL POWER MANAGEMENT CHIPS

MAY 27: 10.14, 52-WEEK RANGE: 6.45 - 14.38, MARKET CAP: 848.63M

Added to the list this month.

Anaheim. It promises to remake Power-One's already strong line of power products; it may remake the company; and it could even impact some of our favorite analog power players. But to understand where Power-One is going, you need to know a little about where they've been.

Beginning in 1973, Power-One was an AC to DC company manufacturing linear analog systems that converted the familiar alternating current of your wall outlet

Through the nineties, Lucent, Ericsson, Power-One, and the tiny SynQor were the chief suppliers of high-end bricks

and the public grid to the direct current used in silicon-based products like computers. In the eighties, the company entered the "switched" power conversion market, making use of new transistor-based technologies to perform AC to DC conversions more efficiently. Then in 1996, as the Telecom was taking off, Power-One shipped its first DC to DC converters, which took a high voltage input and supplied lower-voltage outputs for the range of telecom and computer equipment required to build the Internet. It also started building DC "power plants" to convert 480V AC to 48V DC in order to feed large telecom offices and data farms. But the company is still best known for its DC-DC "bricks," where it has a market share of around 15 percent.

Bricks are the gatekeepers regulating the power entering a printed circuit board or line-card. They take external electricity, often the 48V variety coming from the power plant, and convert it to voltages useful in micro-electronic applications—12V or 5V and down. Bricks also "isolate" the board, guarding against aberrant power swings that could hit connected off-board devices. They confine on-board electrical failures to the board alone.

The original "brick," produced by **Vicor** (VICR) in 1984, measured 4.6 x 2.4 inches—thus its name. Today, technology has shrunk these devices, and they come in half, quarter, eighth, and maybe soon, sixteenth-brick footprints. Through the nineties, **Lucent** (LU), **Ericsson** (ERICY), **Power-One**, and the tiny **SynQor** were the chief suppliers of high-end bricks. Then in 2000, Lucent sold its power operations to industrial conglomerate **Tyco** (TYC), who remains a force in the market today.

In the second issue of their groundbreaking *Digital Power Report* (all issues now available in the *Gildertech.com* archives), Huber and Mills said that Power-One could be the "Cisco of the Powercosm." They wrote that the "rule of thumb for brick demand going

forward" was "at least one brick per motherboard, often a brick per CPU, and bricks for all the other high-speed, board-mounted silicon in all high-power infrastructure applications. High-power bricks stand behind every bit in a central office telephone switch and its accessories; wireless communications equipment; microwave transmitters, receivers, and repeaters; voice processing equipment; PBXs; and internetworking equipment such as hubs, routers, ATMs, and backplanes; the boxes and rack mounts sold by **Cisco** (CSCO), **Nortel** (NT), **Ericsson**, **Lucent**, **Sycamore** (SCMR), **Avici** (AVCI), and **EMC** (EMC)."

Building with bricks was part of a new distributed power architecture (DPA), where power management functions were distributed onto boards and close to big processors, the end consumers of power. As processors proliferated, however, bricks and their attendant circuitry began to crowd circuit boards, all at great cost.

Early in the new millennium, a slightly more sophisticated architecture emerged. Instead of using a brick for each chip requiring a distinct voltage supply, Lucent/Tyco introduced the point-of-load converter, or POL. A POL is essentially a less expensive non-isolated DC-DC brick, fueling big processors with a reliable supply of precision electrons at a desired voltage. Because the primary brick on the board already protects other nearby boards, boxes, and the network, POLs can shed the expensive responsibility of isolation.

POLs, however, have their own unique and difficult tasks. As IC voltages drop, so does their tolerance for power aberrations. A one percent tolerance at 48 or 12 volts is much easier to accomplish than a one percent tolerance at 1.5 volts. POLs must therefore regulate power to the new low-voltage ICs with much greater precision than in the past.

The new architecture using a brick at the "front end" and POLs near each chip on the board was known as the intermediate bus architecture, with the brick feeding the POLs 12V power, and each POL performing the conversion to 3.3V, 2.5V, and so on.

Before long, however, the new analog intermediate bus architecture itself began repeating the complexity of the brick-heavy distributed power architecture. Sprouting up all around the POLs were what Derek Lidow calls "shrubbery," analog devices, passive and active, resistors and capacitors in clusters and patches, temperature sensors, voltage references and current protectors, timing circuits, proliferating "set points" brambled across the board. Then these analog circuits were linked together and back to a central analog system manager, keeping watch over the performance of the POLs.

This is where things stand today. A brick feeds the POLs. POLs regulate energy flowing to the CPUs, ASICs, FPGAs, and DSPs. Myriad analog sensors moni-

tor and regulate the POLs. At the same time, the number of low-voltage digital chips—and therefore POLs—keeps increasing. Circuit boards might have 3, 5, 8, or 10 distinct voltage outputs. One industry veteran reports seeing a board with 14 outputs. An advanced telecosmic circuit board now requires many hundreds of components just to ensure several digital chips get fed the right number of electrons.

As their names imply, however, bricks and POLs are fairly dumb (oh, don't be sensitive, we're making fun of politicians, not people from Poland). Although silicon makes up an ever-increasing proportion of these modular components, bricks and POLs are still mostly hard-wired analog beasts.

A few companies, notably Texas Instruments and Artesyn (ATSN), have joined forces to produce standardized POLs. But the loose alliance does little to relieve the poor telecom line-card designer from his chief concerns: an out of control power budget, hundreds of piecemeal custom devices that need to be stitched together, and tens of vendors just for the power components alone.

Digital analog

Operating in stealth for more than two years, Power-One has now introduced the fruits of a \$50 million program to simplify—radically—advanced printed circuit boards, move board-level power from analog to digital, and reinvent the company's sometimes stodgy power supply business in fabless silicon.

Integrating all the analog sensing, monitoring, and adjusting functionality into its own digital point-of-load converters, known as Z-POLs, Power-One creates a general purpose, integrated, software programmable power environment. Instead of many tens or hundreds of parts, Power-One condenses all board-level power into two: the Z-POL, and the Digital Power Manager.

Key to the system's simplicity and programmability is digital pulse width modulation (PWM) within the Z-POL and a proprietary high-speed bus. PWM is a modulation scheme that can be especially effective at mimicking analog outputs in efficient digital circuitry. Normally a brick or POL is hardwired to a certain output or a narrow range of outputs. Using digital PWM, however, Power-One's new point-of-load converter can be programmed to take any input voltage between 3 and 13.2V DC and supply any output voltage between 0.5 and 5.5V DC.

Where frequency modulation (FM) alters the period of a carrier signal and amplitude modulation (AM) alters the strength, or power, of the signal, PWM works by altering the length, or duration, of square-wave pulses. The percentage of time that the pulse is "on" is said to be the "duty cycle." A pulse that is "on" for three units and then "off" for one unit, then "on" again for three units,

etc., would have a duty cycle of 75 percent. In this way, digital pulses could efficiently alter a bus input voltage of 12V to yield a 9V output. To achieve a 1V output to a state-of-the-art microprocessor, we would choose a digital PWM duty cycle of 8.333 percent (1V/12V).

Exactly similar duty cycles can have different ratios and thus different frequencies. Consider a light bulb whose power is being modified using PWM. If we want a 100W bulb to shine at half its strength, 50W, we would use a 50 percent duty cycle. But if we operate at 10 Hertz, the bulb will appear to flicker, and we will not achieve the desired smooth half-power effect. If we keep the 50 percent duty cycle but increase the frequency to 1 kilohertz, a thousand cycles per second, our eyes will not detect flickering, and the 100W bulb will produce a pleasant 50W.

The frequency of powerchips, POLs included, is important. The rough rule is that a powerchip needs to operate about 1,000 times slower than the chip it is regulating. Thus a 1 GHz processor would require something like a 1 MHz POL. Power-One Z-POLs will have programmable switching speeds of 500 kHz, 750 kHz, or 1 MHz.

Because Power-One has accomplished a fully digital system, it can do things easily and quickly that analog implementations cannot. Through software and a graphical user interface, engineers can program and reprogram

Power-One estimates its system could reduce design time for an advanced board from 8 weeks to 2 days

each Z-POL for any output voltage. They can tell the Digital Power Manager to turn the POLs on and off in proper order. Some of today's high-end chips, it seems, don't like to be turned on in the improper order or powered down in the wrong way. The Digital Power Manager and point-of-loads are connected via a high-speed bus that supports up to 32 Z-POLs. Most other non-programmable custom-built systems can support a maximum of 4 or 8 POLs.

When designing a telecom line-card with analog power components, every experiment or change of plans requires a hardware change. With a digital system, software allows trial and error and no-fault do-overs. Power-One estimates its system could reduce design time for an advanced board from 8 weeks to 2 days. In a typical board design with 8 voltage outputs, the company claims reductions from some 200 components to just 9; from 600 PCB (printed circuit board) traces to just 76; from 10 square inches of PCB space to just 4.4; all at a lower cost.

TI: digital Power-Too?

Power-One achieved much of this breakthrough via its acquisition of a small company called di/dt. The di/dt engineers had designed the first POLs at Lucent, which became Tyco's POLs. The team then broke away until Power-One came along. It had previously acquired IPD, a Tyco competitor, and the source of Power-One's first generation POL. The company claims its innovations will be difficult to replicate because of hundreds of pending patents and because no one else has such expertise in both power conversion and silicon. Power-One always had power smarts, but to execute its stealth strategy over the last two years it had to go out and hire about 95 percent of its silicon talent from other Silicon Valley companies.

Sixty percent of Power-One's current sales come from the communications sector, with industrial, automotive, and semiconductor test equipment accounting for 16, 8, and 6 percent, respectively. Cisco is by far the biggest customer at 16 percent, with Nokia (NOK) trailing far behind somewhere under 5 percent. The new integrated power solution for boards and line-cards is a double-down bet on its current best customers, and it was developed with their intense consultation over the last two years. Power-One thinks it can increase its share of the global POL market of just 1-2 percent today to some 25 percent by 2008. By then it projects the POL market to be about \$3.5 billion, double the size of the slow-growing "brick" market. It thinks it can take 20 percent of the total DC-DC market, which it and industry analysts think will be \$6.3 billion by 2008.

Power-One says although the new system goes on sale later this year we should not expect significant sales from the Z-One architecture until 2006. Today the company's market cap of \$849 million is supported by \$84 million in cash and March quarter sales of \$69 million. It expects slightly higher sales in the June quarter and its currently narrow loss of some \$ 3 million per quarter to turn toward profitability by the September quarter.

Of course, competition is gathering. With its purchase of Power Trends and alliance with Arasan, Aztec, and Emerson (EMR), TI is particularly focused on mas-

tering the intricacies of digital power. Soon to launch an IPO is **Volterra**, a leader in digital power controller components. But developing a complete digital power regulation scheme integrated at the system level, only Power-One has mastered the entire set of skills needed to clear the shrubbery off the board and launch digital power control down a new learning curve, benefiting from Moore's law. It joins our list this month.

—George Gilder and Bret Swanson,
May 27, 2004

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