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The Microcosm Strikes at Cisco City

Broadcom challenges the consensus that communications chips operating at gigahertz speeds require specialized semiconductor processes

In a possibly apocryphal story, the great scientist has just delivered an authoritative presentation on the evolution of the cosmos, all the way up from the Big Bang to entropic heat death. Up from the audience pops a little old lady to ask the professor how he reconciles his depressing theory with the more uplifting and common-sensical idea that the earth in fact is poised gaily and perdurably on the back of a giant turtle. "But Ma'am," the great scientist inquires, "what is it that holds up the turtle?"

The woman responds, "Another turtle, of course."

"And what holds *it* up?" coolly pursues the scientist.

"Oh, don't you see?" the little old lady replies impatiently. "It's turtles all the way down."

Today a new turtle theory has become widely popular in business. Its leading prophet is Clayton Christensen, author of *The Innovator's Dilemma*. In an elaborately developed argument, he shows that low margin, underperforming turtles can sometimes outpace all the high powered hares of international commerce.

The evolution of industries follows a path from vertical to horizontal. As Christensen shows, vertically integrated hares thrive during the period of "undershoot" and innovation, when existing technologies cannot fulfill the needs of customers. To push the technology forward, firms must optimize and customize every interface between components and integrate them together into long legged leading edge systems. **IBM** (IBM) and **Digital Equipment** were the prime examples in earlier phases of the computer industry, making everything from chips to software.

As the industry matures, however, its rabbits, aimed toward high margin customers, tend to overleap the needs of Main Street. Although its low margins are unattractive to the high rollers of leading edge technology, Main Street offers large volumes and will accept products based on off-the-shelf components with sub-optimal but industry standard interfaces. These components and their makers are the turtles of business life. With different companies specializing in different modules, the industry eventually shakes down into a more horizontal structure.

In time the turtle products—think of plastic shelled chips with short-legged metal pins—proliferate at a rate far exceeding the unit totals of the high-end system. The large volumes of the low end items push their producers down a learning curve that ultimately gives them

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higher cost effectiveness and a market expanded by a wider range of software. In the PC industry, the crucial modules, with the largest volumes, were microprocessor CPUs. Profits ultimately migrated from the producers of boxes and systems to the makers of microchips and software, chiefly **Intel** (INTC) and **Microsoft** (MFST).

Nortel, Corning, JDSU ...

Today the network is king, and the same dynamics apply. The rise of the turtles in this huge domain is obscured by the division of the network equipment industry between an embryonic all optical branch and a maturing electronic branch. But if you listen to the technology, as Carver Mead advises, you can already detect the voice of the turtle tolling through the realms of Cisco City, where chip makers are gathering to capture the profits of the lord of the hares.

Network backbone profits migrate first toward the makers of optical equipment, such as vertically integrated **Nortel** (NT), **Corning** (GLW), and **Lucent** (LU), and then toward their suppliers such as **JDS Uniphase** (JDSU) and **Avanex** (AVNX). With the optical industry still in its infancy, vertical and horizontal strategies will prosperously coexist for a decade or so. Pushed inexorably toward the edge by the all optical mandate will be all the electronic routers and switches and protocol converters that are now dispersed through the rabbit warrens of both telephone and data networks.

The good news for **Cisco** (CSCO) is that unit demand for routers will continue to expand explosively. The bad news is the hollowing out of the router and its dispersal across the fringes of the network. Routers will make their way into homes, shops, and apartments, into PCs, into settop boxes, into cable and digital subscriber line (DSL) modems, into company hubs, into wireless ports, into voice-over-IP processors, into multimedia gateways, into servers, and into automobiles. A router, however, will no longer be a hare but a turtle, not a box but a chip. The profits will migrate toward the makers of "network processor" chips, who will compete for the role of the Intel of the network edge.

A treacherous and complicated place, where light and electricity converge, with tricky patterns of interference and marketing, the network edge is partly the domain of crafted analog devices created by optical component producers such as JDS Uniphase and its rivals. Prominent among these units on one side of the fibersphere are the lasers that transmit an infrared beam, the external modulators that shape the signal, and the multiplexors that empower WDM. Ultimately these signals will flash through an all optical network. On the other side of the fibersphere, to receive the signal, are filters and demultiplexors that break the beam into lambda bitstreams, photodetectors that sense the lambda and convert it to a tiny stream of electrical pulses, and transimpedance and parametric amplifiers that convert it into a readable voltage. Requiring low noise operation and exquisite sensitivity, these devices are custom made by companies such as **Conexant** (CNXT) and **RF Micro Devices** (RFMD) using semiconductor processes such as gallium arsenide, indium phosphide, and other bipolar heterojunctions, sometimes in packages bearing a single transistor.

Once the signal has been sensed and amplified, however, it leaves the analog domain of single transistor devices and enters the world of digital microelectronics with scores of millions of transistors in a single chip. Following the amplification stages that prepare the signal for digital processing come the physical layer chips that translate the analog voltages into a stream of bits and then the framers that shape them into packets—the envelopes which hold the message for transport and bear its address. After the packet is framed, it enters the complex digital gantlet of network processing: the packet parsing, classification, lookup, address resolution, modification, routing, and switching that comprises the Internet at layers two and above. At the end of this electronic trek, the signal may be processed by drivers for the lasers and reenter the fibersphere.

... chase Cisco to the edge

Until recently, the array of digital functions was chiefly done in application specific integrated circuits (ASICs) that are optimized for a single job and take as long as two years to develop. But over the last couple years the movement of the networking industry toward Internet time has led to the introduction of generic programmable devices for these purposes resembling Intel's programmable microprocessors that took over the computer industry.

One of the many contenders for this role is…Intel itself, with its purchase of **Level One** (meaning physical layer) and Digital Equipment's semiconductor division in Hudson, Massachusetts. Intel has released a network processor family called IXP1200 and has gained some 60 low to mid performance design wins. Never underestimate Intel. But in this field the company seems to command no advantages comparable to its imperial x86 microprocessor instruction set. Its world-beating wafer fabs are almost entirely devoted to manufacturing Pentiums. Relegated to an old 0.3 micron plant inherited from Digital Equipment is the network processor product. Meanwhile, from Israel to Irvine is erupting a huge array of network processor companies.

The network processor is to Cisco routers what the microprocessor was to IBM mainframes—a modular and programmable product that incorporates most of the hardware functionality of your equipment. At first, like the microprocessor before it, the network processor will seem radically inferior to your industry leading boxes joining scores of hardwired application specific integrated circuits (ASICs). Custom designed for a single networking task, ASICs can process packets at wirespeed, reading IP addresses, looking up routes, modifying headers, and remitting them to the network in under 100 nanoseconds. Cisco routers assemble these devices into an elegant system architecture with industry standard and proprietary software. Soon to handle terabits per second, these routers can play everywhere from the

pullulating core of the network to its proliferating edges. They can propel Cisco to the world's largest market cap.

The router, however, faces relentless attack from two sides. In the central office and network core, the all-optical cross-connect, arraying thousands of dumb mirrors indifferent to protocols and bit rates, renders even the terabit router an archaic curiosity. On the edge of the network, the programmable network processor—soon to operate flexibly at all seven layers of the networking stack—disrupts and displaces the stand alone router.

For the next generation of microchips, afflicted with a scarcity of silicon area and power, the GTR since 1996 has been upholding a paradigm of programmable single chip systems with parallel processors and broadband on-chip links to embedded Dynamic Random Access Memory (DRAM). In every component, these single chip systems are inferior to the multiple discrete ASICs and attached static RAM memories that they displace. But the stresses of ten gigabit wirespeed networking are bringing forth a new generation of horizontal innovators. Static RAM cells, for example, though using four to six times more transistors per bit than one-transistor DRAM cells, operate some ten times faster. But DRAMs are far denser and fit better on the same chip, where on-chip buses function hundreds of times faster than the few off-chip pins soldered on computer backplanes containing miles of wire afflicted with lightspeed delays. In networking, the lady might be right after all: It will be turtles all the way down.

From the beginning, the cry of the turtle, "Low and slow wins the race," has been the watchword of the chip business. It has combined inferior slow and low powered devices on single chips that outperform heroic aggregations of high powered fast devices. The first integrated circuit cobbled together by Robert Noyce and Gordon Moore at Fairchild used silicon transistors, capacitors, and resistors far inferior to the discrete versions deployed by the Air Force and other high performance customers of the day. Put together on a single chip and manufactured in the millions, these low and slow devices soon far outperformed all rivals.

Xilinx and Qualcomm chip along

The ultimate in low and slow silicon was the complementary metal oxide semiconductor (CMOS) process. A genuine invention, it reduced the power consumption of semiconductors tenfold or more by essentially switching voltages rather than currents, which drain power. Rather than using one kind of transistor, whether negative or positive (NMOS or PMOS—the old Intel fortes), CMOS pairs both kinds of transistors throughout a device, tying the two to a single input in each cell. A negative input voltage that will turn on a P channel transistor will choke off an N channel transistor, and vice versa. Therefore the combination of N and P devices in each cell means that one transistor is always off. Thus, power can flow through the system only in tiny spurts as the devices switch, giving CMOS its uniquely low power consumption. Like a canoe paddled on only one side at a time, a densely laid out CMOS chip both requires less power and causes less disturbance (heat) than rival technologies.

Just as you can run a lot more canoes on a lake than motorboats, you can pack more CMOS devices on a chip. As Carver Mead was first to point out, the smaller devices could be placed closer together, allowing the signals to reach their destinations faster and cooler than signals traversing longer distances. Bumping along the crystal lattice of the material, fast, high powered signals may end up hotter and slower than signals that approach the mean free path of electrons in silicon. *The less the space the more the room*. Various hybrid structures rose up to challenge the basic complementary metal oxide semiconductor (CMOS) standard for some exotic niches. But 98 percent of the market remained with CMOS, allowing the bulk of wafer fabrication to be standardized and relegating the exotic processes to the fringes of the industry. (Granted: one of these fringes turned out to be optics—the ever expanding core of the Internet).

Broadcom's Nicholas is insinuating his products into every nook and niche of Cisco City

In electronics, the dominance of CMOS enabled the fulfillment of Carver Mead's original paradigm for the structure of the semiconductor industry itself. In the 1970s, he predicted that the industry would eventually break down into two parts—fabless chip design houses, on the one hand, and foundries that focused on wafer fabrication, on the other. This split could not happen until chip production was routinized, so that nearly all designs were produced in one way, namely CMOS. With fabless revenues growing nearly 50 percent faster than the overall industry, Mead's prophecy is coming true today. Among our own Telecosm companies, Henry Nicholas's **Broadcom** (BRCM) epitomizes the trend. Surging 164 percent, nearly all from internally generated revenues rather than acquisitions, Broadcom was the fastest growing major U.S. chip company in 1999.

Also fabless were the fifth fastest grower, field programmable gate array star **Xilinx** (XLNX), and **Qualcomm** (QCOM) the sixth. Qualcomm was also number one in total fabless revenues. Among the most profitable firms in the industry were Taiwanese foundries TSMC (**Taiwan Semiconductor Manufacturing Company** [TSM]), and UMC (**United Microelectronics**), with TSMC investing $4.4 billion in new capacity this year, nearly double its last year's revenues. According to In-Stat, foundries will account for some 44 percent of the $8.6 billion of spending slated for new plants in 2000. But with a capacity crunch in view and new fab projects announced daily everywhere from Seoul to Penang, foundries may well do more than half of all greenfields projects.

Atmel and RF Micro's exotic dance

It is Broadcom's Nicholas, however, insinuating his products into every nook and niche of Cisco City, who is most arrestingly bringing the law of low and slow to the high speed arena of broadband. Riding this Mead para-

A STOREWIDTH STORY

The explosive growth of the network and the faster than Moore's Law multiplication of bandwidth have dictated massive growth in demand for storewidth (Chart 1), the ability to move and share large amounts of heterogeneous stored material rapidly on the net.

But as of today, nearly 80 percent of data storage fails the storewidth test, remaining isolated in traditional direct server attached storage arrangements.

Storage Attached Networks (SAN) and Network Attached Storage (NAS), today's generally accepted storewidth solutions, still hold respectively just 19 and 2 percent of the storage market share. Translation: The storewidth bounty is yet to be harvested.

Outside of North America, for instance, SAN solutions are just beginning to take root (Chart 2), and NAS is a mere seedling, a reflection of the overseas lag in network expansion and Internet growth. EMC (EMC), the worldwide dominator of the SAN market, reports only 39 percent of revenues from overseas. As the rest of the world comes on line, storage demand will become storewidth demand (Chart 3).

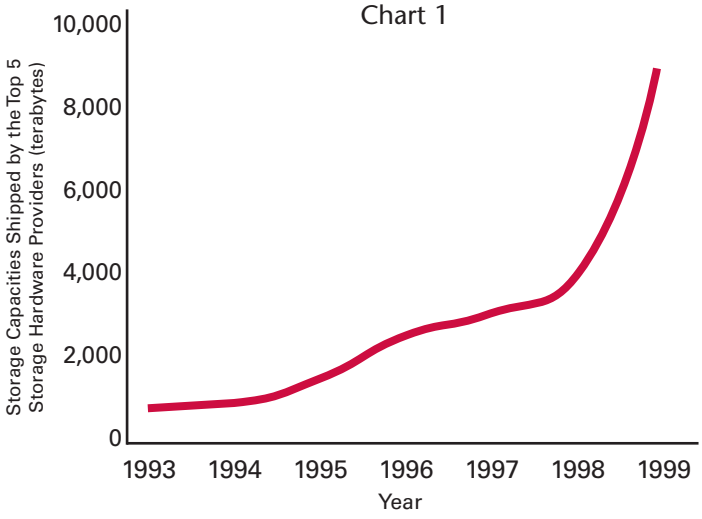
For close to a decade, storage hardware prices have declined as storage capacities soared (Chart 4). Price elasticity is an astonishing 4.0, meaning that for every 1 percent drop in storage hardware costs, storage demand increases 4 percent. The price of IT staff, however, is not in decline (Chart 5). In the U.S. the average full time IT staffer reaps $66K (non Internet companies) to $80K (Internet companies) per year. Personnel costs included, the Yankee Group estimates the total cost of storage management to be as high as $12 per megabyte per year.

Those costs, along with the challenges of accelerating storewidth capacity, have motivated enterprises to outsource and consolidate many of their storewidth management functions. Storewidth specialists including Exodus (EXDS) and GlobalCenter, and their crucial vendors, Sun, Novell (NOVL), Procom (PRCM), Network Appliance (NTAP), EMC, Mirror Image (XLA), along with Storage Service Providers (SSPs) such as Storage Networks (STOR), will prosper by enabling companies to outsource management headaches and cut costs even as they boost their storewidth capabilities and accelerate access across the network (Chart 6).

— Mary Collins

Despite widespread deployment of storage solutions ...

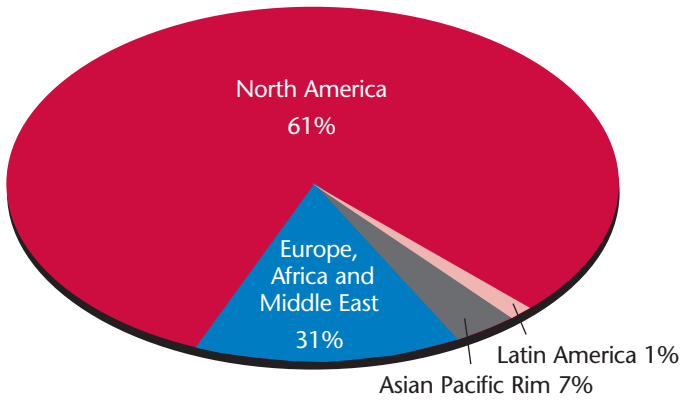
Chart 1



... overseas deployment remains low.

EMC Overseas Sales Revenue in 1999

Chart 2



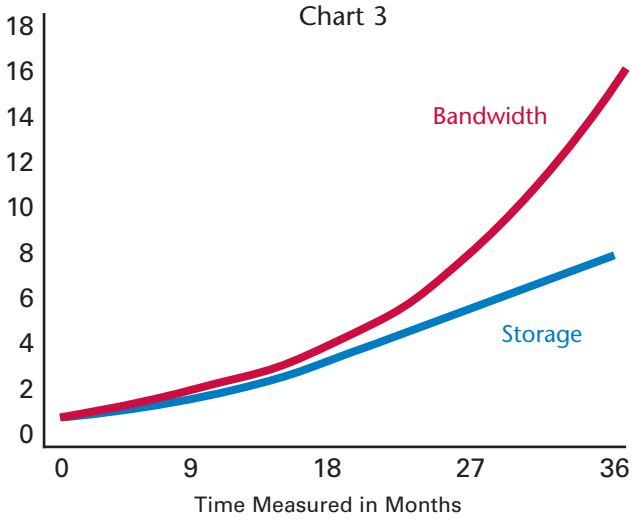
digm, Nicholas is challenging the consensus in the industry that communications chips operating at gigahertz speeds require specialized hybrid semiconductor processes. For some functions this is true. Lasers and amplifiers for high-end optics and wireless, for example, do have to be made in materials with intrinsic band gaps that fit the frequency of the light or the microwave. Seeing this fact, most of Broadcom's rivals, such as IBM, Intel, Conexant, and RF Micro Devices—an exemplary Telecosm player now partnering with both Qualcomm and **Atmel** (ATML)—command exotic fabrication facilities. They readily push into new processes such as copper interconnects and silicon on insulator. Similarly, companies such as **Cree** (CREE) and **Sterling**—turning to silicon carbide for harsh environments in automobiles, airplanes, and industry—discover that their arcane materials also offer benefits in high power, high speed communications.

Yet using "low and slow" CMOS, Broadcom commands between 90 and 100 percent market share on many of the important chips on the edge of the fibersphere, such as gigabit Ethernet transceivers in the enterprise and cable modem processors and settop box engines. How does Nicholas do it?

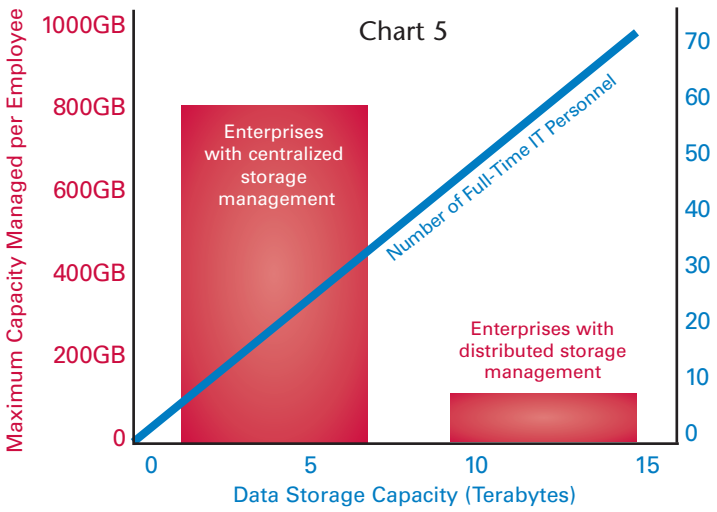
He uses the Microcosm paradigm. Rather than starting with the demand for high frequencies and figuring out how to change the silicon to deliver them, Broadcom begins with the necessity of cheap CMOS as a given. To create cheap high volume products you must use the cheap high volume process available in the foundries. Then Broadcom's designers figure out what else has to be changed to deliver high frequencies.

This CMOS necessity has mothered a series of clever circuit level inventions that simplify computations and render them manageable on the generic silicon processes. Once the hardest parts of the design are adapted to CMOS, they can

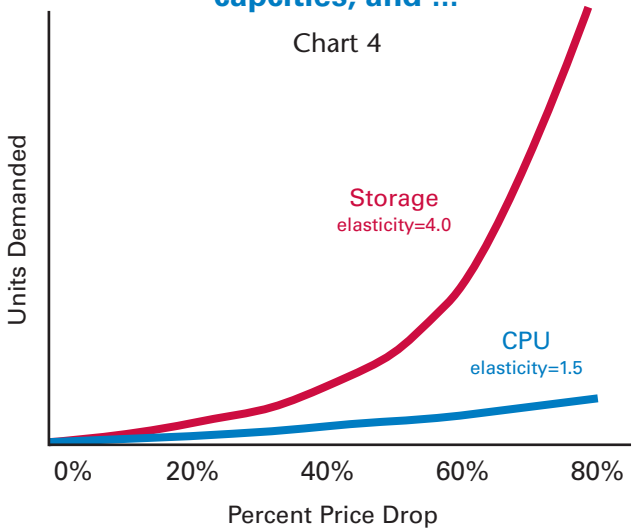
Surging bandwidth growth...



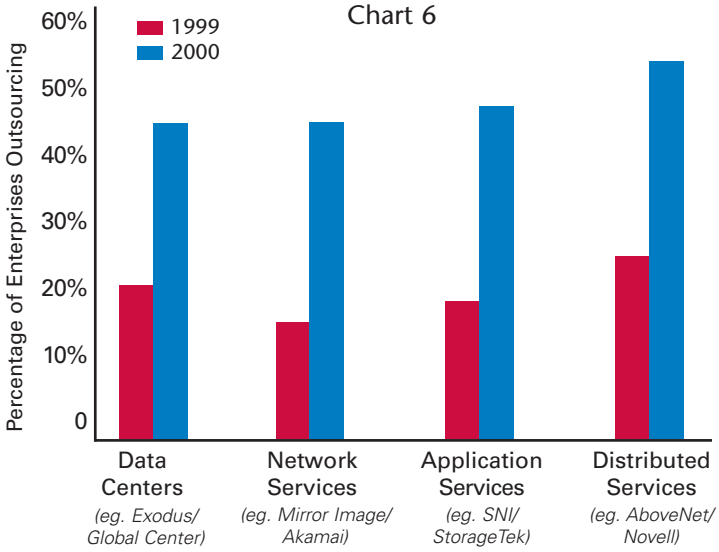
... the rising cost of storage management ...



... has induced growth of storage capcities, and ...



... has reshaped the storage outsourcing market.



Sources: The Holy Grail of Data Storage Management, Jon William Toigo; EMC; InfoWorld

be combined on the same chip with other digital functions. Through ever more impressive feats of integration, the company is incorporating an array of new features on these networking chips, including Universal Serial Bus and Firewire links, TCP-IP ports, Motion Picture Experts Group (MPEG) image decoders, firewall protection, and encryption for e-commerce. It also plans to integrate functions that turn the internal phone lines in your house into a 38 megabit per second network reachable through an ordinary phone jack in the wall and transform all your appliances into portable Bluetooth accessories.

Broadcom spices things up

Broadcom has even announced the first 10 gigabit Ethernet transceiver on a single chip. Dwight Decker of Conexant, the proud proprietor of leading edge fabs in gallium arsenide, bipolar heterojunctions, and silicon germanium, points out that the Broadcom device in fact bonds four 2.5 gigabit per second channels together. The first one channel 10 gigabit Ethernet transceiver and the only OC-192 chip both came from **Applied Micro Circuits** (AMCC) on silicon germanium. But why carp? No matter how well some other firm with a fancy fab can perform some of these functions, it will not be able to compete with Broadcom's integrated product salable for under $50.

Including hundreds of PhDs and the CEOs of 12 acquired companies, Broadcom's engineers are some of the leaders in the industry. Now Broadcom is adding to its lead in leaders by purchasing **Silicon Spice**, a company headed by former Pentium and then **Advanced Micro Devices** (AMD) K-6 design team chief Vinod Dham. Conserving silicon, the company creates reconfigurable chips for gateways

to transform IP packets into multiple parallel bit streams to deliver voice, video, or other web functions, or to convert these multimedia bit streams into IP packets to be sent over the network. Critical to transforming the world's billions of plain old telephone lines into multimedia Internet channels, such gateway chips push Broadcom ever deeper into Cisco's path.

Broadcom's strategy has been unfolding step by step, gigabuck acquisition by gigabit innovation, day by day through the summer. Following hard on the purchase of Silicon Spice came the portentous acquisition in mid-August of **NewPort Communications**. NewPort's elite team of process designers, attired in simple plastic, are coming after the feudal armies of exotic chip makers, clad in ceramic armor packages with costly gills to shed the heat.

Conexant is the only company with products for all cellular and PCS standards, Bluetooth, MMDS, and LMDS devices

Founded by two key designers from Conexant, Armand Hairapetian and Lorenzo Longo, NewPort is an innovator in advanced CMOS processes that it terms current-controlled C^{3}MOS. The key problem of CMOS in communications is that at high frequencies it begins behaving like a watt hungry bipolar device, spending most of its time switching between positive and negative, gushing current, catastrophically losing its power efficiency.

As a result, the frequencies on CMOS microprocessors from Intel, **Sun** (SUNW) and AMD are topping out at a little over one gigahertz, while some communications processing functions must run at frequencies in the scores of gigahertz to deal with multiple OC-192 and 10 gigabit Ethernet streams. NewPort's C^{3}MOS process uses clever circuit design to raise transistor cut off frequencies as high as 60 gigahertz compared to 45 or 50 gigahertz in silicon germanium. This breakthrough enables creation of leading edge communications processors on ordinary CMOS foundry fabs in Taiwan. The showcase product is a one channel 10 gigabit Ethernet transceiver on two chips. Being moved toward a single device, it may cost less to produce than the AMCC product's packaging alone.

Conexant covers wireless

The GTR has a large stake in this struggle because we have been maintaining for some four years that new communications chips will require silicon germanium, an adaptation of CMOS which enables a better tradeoff between power usage and speed than gallium arsenide. Silicon germanium can use most of the same equipment as ordinary CMOS processes. But it requires additional steps of exotic high pressure chemical vapor deposition to lay down the germanium base for the transistors, and it entails a different transistor structure. For some critical devices it is worth the trouble, as is the radically different gallium arsenide.

A fabless company lacking these specialized processes, Broadcom has necessarily shunned most microwave and cellular wireless markets. Yet these promise some of the largest returns in the next decade. Conexant may not have kept up with Broadcom in the household and enterprise network arena, but its several wafer fab processes have served it well in the wireless arena. It is the only company with products suitable for all the cellular and PCS standards, Bluetooth single chip transceivers with a ten meter range, and MMDS at 2.4 gigahertz and LMDS devices at 28 to 38 gigahertz. These can be huge markets. Some of them are also being targeted by Qualcomm, which is spinning off its chip firm to compete more aggressively in this crowded arena where it commands much of the crucial intellectual property for the 3G era.

Nicholas is also pursuing Bluetooth, a 700 kilobit link manufacturable in CMOS, as a way to link settop boxes and other networks wirelessly to PCs within the home. But wireless is a scarce bandwidth and often specialized fab play, and Broadcom is all about broadband on generic CMOS. Its goal is to join together all the functions of network processors, content addressable switch fabrics, and communications gateway processors in increasingly integrated CMOS systems on a chip.

Motorola & MMC Networks kick up sand

Nonetheless, still conspicuously missing from the Broadcom panoply is perhaps the most important element of all. From the last InterOp in Las Vegas in May to Hot Chips in San Jose in August the highest hopes have focused on "network processors." In conjunction with switch fabrics, network processors perform most of the essential functions of routers and gateways. Currently being pursued by scores of aggressive companies on Internet time, these devices are rendered on many different substrate materials, chief among them dynamically reconfigurable PowerPoint slides or application specific ink on glossy bond. But they ultimately must classify, filter, parse, modify, frame, or stream the onrush of data at wirespeed. Wirespeed, unfortunately, refers not to the monthly publication schedule of the eminent digital lifestyle journal but to the pace of fiber optic communications at 10 million packets a second or 10 gigabits per second per lightpath.

"Where is the Sand?" headlined the *Electronic News* report on the August San Jose Network Processor 2000 conference. As it turns out, most of the silicon is currently being kicked up by Intel, by **MMC Networks** (MMCN) (now being purchased by AMCC of the Telecosm list), by the Maker division of Conexant (also Telecosmic), and by **Motorola** ([MOT] ditto). With some 4000 design wins, Motorola is outpacing Intel in this field and annually sells more than a billion dollars worth of Power PC chips adapted to network processing applications. Motorola has just purchased C-Port, also silicon short but software savvy in the network processor arena, promising devices that operate at up to 10 gigabits per second.

The company with by far the best PowerPoints and acoustics, however, is **EZchip** of Migdal Haemark in Israel, which manages to hit nearly all the paradigm buzz buttons at once with one set of 29 slides. It uses a heavily parallel and pipelined architecture with 64 programmable datapaths that it calls TOPs (task optimized processors), all integrated on a single chip. Each TOP spins one of the key network device functions, including parsing (or classifying), searching, resolving, and modifying packets. Under CEO Eli Fruchter, it promises wirespeed at 10 gigabits a second for all seven network layers—including access control, accounting, web page switching, content addressing, load balancing, service level agreement guarantees, voice over IP and video broadcasting.

EZ does it

Even using configurable PowerPoint substrates, these are all awesome claims. At 10 gigabit wirespeed, the time to process each packet is just 60 nanoseconds. Off-chip DRAM takes 60 nanoseconds for just one fetch. Fruchter's solution is the paradigm. Avoiding the speed of light delays necessarily entailed by off-chip memory, he uses low and slow on-chip CMOS DRAM with very wide (256 to 512 bit) buses to the processors that yield a total memory bandwidth of 500 gigabits per second. To achieve the applications layer content searching and switching, EZchip has developed five patented search algorithms that reduce by tenfold or more the number of memory fetches.

Early next year, the chip will be transferred from PowerPoint to tapeout to be manufactured in 0.18 micron CMOS at "the world's leading foundry" according to Fruchter. In August, the company's 60 Israeli engineers completed the coding of the chip design in VHDL (Visic hardware design language). Although any bet on slideware may slip, the many eager candidates to design in EZchips are said to include the top networking equipment companies.

EZchip seeks to usurp first generation network processors that integrate several off-the-shelf RISC (reduced instruction set computing) machines on a chip and couple them to separate co-processors. General purpose devices, RISCs cannot delve deep into packets. Other net processors use a mix of RISCs and ASICs, charging the RISC with the core processor tasks and the ASICs with specific high-speed jobs. ASICs add to the number of chip interfaces and by definition are not programmable. All first generation net processors use off-chip memory, imposing a 32- or 64-bit limit on the links—the buses—between processor and memory.

Five megabytes of on-board DRAM (2 MB for the buffer and 3 MB for searching) and buses as wide as 512 bits mean EZchip can go beyond reading simple headers in network layers 2-4 and deep into the strings of text-based data in layers 5-7. Processing layers 5-7 is essential for such functions as server load-balancing and per-use accounting of web-based video or software applications.

Scalable and cascadeable, EZchip's first product, the NP-1, can process eight ports of 1 gigabit Ethernet, one port of 10 gigabit Ethernet, or one port of OC-192 SONET. Samples will be available next spring, with volume shipments by summer.

EZchip's team comes from the networking industry rather than the chip industry. Their previous project implemented Token Ring networks, which were elegant in concept but succumbed to the superior robustness and momentum of Ethernet. With a focus on 10 gigabit Ethernet, this time they have got it right, conceiving a perfect device to reduce the router to a chip and put it everywhere. Even though the company is 78 percent owned by a rapidly shrinking supplier of firewall technology called **LanOptics** (LNOP), we promote it to our list.

The EZchip architecture does not include an onboard switch fabric. The leading producer of switch fabrics is MMC Networks. But one of the most innovative devices in the switch fabric arena is Broadcom's content addressable matrix enabled by last year's Maverick acquisition. A content addressable switch fabric can operate at layer seven, the application layer, and allow a device to treat different packet contents in different ways at wirespeed, filtering out porn, for example, or enforcing access rules. Broadcom's initial use of the Maverick device was in the Local Area Network, where Cisco is a leading customer. But like most of the Broadcom devices the chip is being adapted to all the multifarious gateways in the wide area as well. Combined with the Silicon Spice broadband IP gateways, the NewPort 10 gigabit transceivers, and whatever network processor chip—hard or easy—Broadcom ultimately buys or contrives, the switch fabric pushes the company deep into Cisco territory. As these devices get integrated onto single CMOS chips, Cisco will probably continue to purchase them in ever greater numbers. But in time they will comprise most of the value of router hardware. Cisco will become a box assembler like **Dell** (DELL). Soon enough the router will go away. It will become a Broadcom or an EZ chip.

EZchip will reduce the router to a chip and put it everywhere

A rough rule of the Telecosm ordains that hardware softens on the edge of the network and software hardens at its center. The network processor represents a software intensive router. As John Chambers sometimes seems to recognize, the likely outcome is that Cisco will retreat from its hardware revenue addiction to a role as a networking mutual fund and a software bastion of intellectual property. Already most of the value of Cisco boxes resides in software: its Internet Operating System, Border Gateway Protocol, its Open Shortest Path First algorithms and all the other code structures that underlie most of current Internet architecture. A street map of Cisco City, this is a rich vein indeed. But what happens when the vein turns into glass?

George Gilder & Richard Vigilante
September 6, 2000

TELECOSM TECHNOLOGIES

ASCENDANT TECHNOLOGY **WINGS OF LIGHT**	COMPANY (SYMBOL)	REFERENCE DATE / PRICE		AUG '00: MONTH END	52 WEEK RANGE	MARKET CAP
Wireless, Fiber Optic Telecom Chips, Equipment, Systems	Lucent (LU)	11/7/96	11 25/32	41 213/256	39 5/8 - 84 3/16	139.7B
Wave Division Multiplexing (WDM) Systems, Components	Ciena (CIEN)	10/9/98	8 9/16	221 11/16	29 3/8 - 214 9/16	31.5B
Wireless, Fiber Optic, Cable Equipment, Systems	Nortel (NT)	11/3/97	11 1/2	81 149/256	19 7/8 - 89	242.8B
Optical Fiber, Photonic Components	Corning (GLW)	5/1/98	40 15/16	327 245/256	62 5/8 - 340	96.4B
Wave Division Multiplexing (WDM) Components	JDS Uniphase (JDSU)	6/27/97	3 5/8	124 31/64	25 13/16 - 153 3/8	97.4B
Adaptive Photonic Processors	Avanex (AVNX)	3/31/00	151 3/4	151 15/32	47 3/8 - 273 1/2	9.7B
All-Optical Cross-Connects, Test Equipment	Agilent (A)	4/28/00	88 5/8	60 85/256	38 3/16 - 162	27.3B
THE LONGEST MILE						
Cable Modem Chipsets, Broadband ICs	Broadcom (BRCM)	4/17/98	6*	250	51 9/16 - 274 3/4	55.5B
S-CDMA Cable Modems	Terayon (TERN)	12/3/98	15 13/16	55 1/2	15 5/8 - 142 5/8	3.4B
Linear Power Amplifiers, Broadband Modems	Conexant (CNXT)	3/31/99	13 27/32	37 3/16	26 1/2 - 132 1/2	8.5B
THE TETHERLESS TELECOSM						
Satellite Technology	Loral (LOR)	7/30/99	18 7/8	7 21/32	5 - 25 3/4	2.3B
Low Earth Orbit Satellite (LEOS) Wireless Transmission	Globalstar (GSTRF)	8/29/96	11 7/8	9 7/8	5 13/16 - 53 3/4	957.0M
Code Division Multiple Access (CDMA) Chips, Phones	Qualcomm (QCOM)	7/19/96	4 3/4	59 7/8	38 1/16 - 200	44.6B
Nationwide CDMA Wireless Network	Sprint (PCS)	12/3/98	7 3/16 *	50 53/256	29 - 66 15/16	46.6B
CDMA Handsets and Broadband Innovations	Motorola (MOT)	2/29/00	56 53/64	36 21/256	27 5/16 - 61 1/2	78.7B
Wireless System Construction and Management	Wireless Facilities (WFII)	7/31/00	63 5/8	75	30 5/8 - 163 1/2	3.2B
THE GLOBAL NETWORK						
Broadband Fiber Network	Level 3 (LVLT)	4/3/98	31 1/4	86 1/16	49 7/8 - 132 1/4	31.5B
Broadband Fiber Network	Metromedia (MFNX)	9/30/99	12 1/4	39 15/16	11 1/8 - 51 7/8	21.9B
Submarine Fiber Optic Network	Global Crossing (GBLX)	10/30/98	14 13/16	30 1/16	20 1/4 - 61 13/16	26.5B
Broadband Fiber Network	Northeast Optic (NOPT)	6/30/99	15 1/16	44 7/16	27 7/8 - 159	740.2M
Telecommunications Networks, Internet Access	WorldCom (WCOM)	8/29/97	19 61/64	36 1/2	32 9/16 - 61 5/16	104.9B
CACHE AND CARRY						
Directory, Network Storage	Novell (NOVL)	11/30/99	19 1/2	12 1/4	7 7/8 - 44 9/16	4.0B
Java Programming Language, Internet Servers	Sun Microsystems (SUNW)	8/13/96	13 3/4	126 15/16	37 1/2 - 128 5/8	201.8B
Network Storage and Caching Solutions	Mirror Image (XLA)	1/31/00	29	18 7/8	1 13/16 - 112 1/2	2.0B
Disruptive Storewidth Appliances	Procom (PRCM)	5/31/00	25	48 1/4	6 1/8 - 89 3/4	550.9M
Remote Storewidth Services	Storage Networks (STOR)	5/31/00	27*	101 1/2	82 - 154 1/4	9.2B
THE MICROCOSM						
Analog, Digital, and Mixed Signal Processors	Analog Devices (ADI)	7/31/97	11 3/16	100 133/256	23 5/16 - 100	35.7B
Silicon Germanium (SiGe) Based Photonic Devices	Applied Micro Circuits (AMCC)	7/31/98	5 43/64	202 15/16	22 5/8 - 200 1/2	25.5B
Programming Logic, SiGe, Single-Chip Systems	Atmel (ATML)	4/3/98	4 27/64†	20	7 1/2 - 30 11/16	9.2B
Digital Video Codes	C-Cube (CUBE)	4/25/97	23	23 1/4	14 1/4 - 106 1/4	1.1B
Single-Chip ASIC Systems, CDMA Chip Sets	LSI Logic (LSI)	7/31/97	15 3/4	36 5/16	21 9/16 - 90 3/8	11.3B
Single-Chip Systems, Silicon Germanium (SiGe) Chips	National Semiconductor (NSM)	7/31/97	31 1/2	44 1/2	23 1/2 - 85 15/16	7.9B
Analog, Digital, and Mixed Signal Processors, Micromirrors	Texas Instruments (TXN)	11/7/96	5 15/16	66 245/256	37 7/8 - 99 3/4	109.8B
Field Programmable Gate Arrays (FPGAs)	Xilinx (XLNX)	10/25/96	8 7/32	88 7/8	30 1/2 - 98 5/16	29.2B
Seven Layer Network Processors	EZchip (LNOP)	8/31/00	16 3/4	16 3/4	3 3/8 - 43 3/4	108.1M

ADDED TO THE TABLE: EZCHIP

† SPLIT ADJUSTED THIS ISSUE

* INITIAL PUBLIC OFFERING

NOTE: The Telecosm Table is not a model portfolio. It is a list of technologies in the Gilder Paradigm and of companies that lead in their application. Companies appear on this list only for their technology leadership, without consideration of their current share price or the appropriate timing of an investment decision. The presence of a company on the list is not a recommendation to buy shares at the current price. Reference Price is the company's closing share price on the Reference Date, the day the company was added to the table, typically the last trading day of the month prior to publication. Mr. Gilder and other GTR staff may hold positions in some or all of the stocks listed.

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